

REMARKS

INTRODUCTION

In accordance with the foregoing, claims 1, 3, 4, 7, 9 and 14 have been amended. Claims 2, 5, 6, 10 and 15 have been cancelled. Claims 1, 3, 4, 7-9 and 11-14 are pending and under consideration.

CLAIM REJECTIONS

Claims 1 and 4-8 were rejected under 35 USC 102(b) as being anticipated by Becerra et al. (US 5,917,509) (hereinafter "Becerra").

Claims 2 and 3 were rejected under 35 USC 103(a) as being unpatentable over Becerra in view of Edelen et al. (US 6,547,356) (hereinafter "Edelen").

Claims 9-15 were rejected under 35 USC 103(a) as being unpatentable over Becerra in view of Edelen and Morita et al. (US 6,511,160) (hereinafter "Morita").

Becerra

Becerra discloses a method and apparatus for interleaving pulses in a liquid recorder. In Becerra, the data management and power pulse scheduling functions are accomplished by major circuit elements. A system controller 67 accepts from an image source on line 160, a system user interface on line 162, such as a user panel or soft display interface, and one or more auxiliary control factor sources on line 164, for example a temperature sensing and control system or an input media monitoring system as well as other signals for managing the total operation of the liquid recording apparatus. The overall system controller 67 provides the remaining circuitry with signals conveying data on line 71, direction of printing, also on line 71, data bit shift clocking on line 77, drop emission timing (ENABLE signals) on line 73, and logic circuit reset on line 75. The system controller 67 also manages the burn voltage power supply 66 on line 79. The data is entered via a DATA/DIRECTION LINE 71 in four bit serial fashion where it is latched by 4-bit serial data latch 82. At the proper time, controlled by the load clock, LCLK, the four bits of data are transferred and latched to the 4-bit parallel data latch 80. The LCLK signal as well as the other timing signals PHASE A, PHASE B, SCLK N, and SCLK P are generated by the timing generator circuit 86. The function of the timing generator circuit 86 is described in detail below. The data is further controlled by a set of four logical AND gates 78, which all have an additional logical input, the PHASE B signal. Therefore, only if the PHASE B signal is high will the four bits of data be presented to the inputs of four logical OR gates 76 and

subsequently appear on the four data lines 94. Becerra, 6:65-8:27 and Figure 7.

In Becerra, there is provided a signal PHASE A as an output from timing generator circuit 86, which can also be presented to all of the logical OR gates 76. This PHASE A signal is not controlled by the data, but, if presented to the logical OR gates 76, will be passed out to all of the data lines 94. Therefore, the predrivers 74 receive logical inputs from the data lines 94 for either the case of PHASE B AND DATA being high (logically true) or PHASE A being high (logically true). By controlling the timing relationships of PHASE A and PHASE B, the predrivers 74 can thus receive two power pulse commands, one which is the same for every emitter of the emitter bank 96 and derives from PHASE A, and a second which is controlled in time by PHASE B but is given only for emitters which also have DATA logic highs. Becerra, 7:28-7:42 and Figure 7.

In Becerra, the timing generator circuit 86 provides the signals: LCLK, PHASE A, PHASE B, SCLK N, and SCLK P. The LCLK causes the 4-bit parallel shift register 80 to latch whatever data is held by the 4-bit serial shift register 82. The PHASE A signal allows all of the emitters of an emitter bank 96 to receive power if the bank's bank selection line (F1-F32) is currently held high by the bank selection shift register 90. The PHASE B signal allows each of the emitters of a bank of emitters 96 to receive power if the data line 94 for the emitter is high and the bank's bank selection line (F1-F32) is being held high by the bank selection shift register 90. Shift clock signals SCLK N and SCLK P are non-overlapping logical inverses of each other and cause the bank selection shift register to advance a token bit thereby shifting the selected bank of emitters 96 along the 32-bank row. The bank selection shift register 90 operates bi-directionally so that the banks of emitters 96 can be selected in opposite order for printing in bi-directional carriage printer fashion. Becerra, 8:41-8:59.

The timing generator circuit 86 derives its output signals from the logic input on the ENABLE LINE 73 and the non-overlapping logical inverse of the signal input on ENABLE LINE 73, both are provided by the non-overlapping signal generator 84, and from the signal input on the FUNCTION CLEAR LINE 75, which serves to logically reinitialize the timing generator circuit 86 at the beginning of each printing cycle. Both the ENABLE and the FUNCTION CLEAR signals are provided by an overall printer system controller 67. The timing generator 86 is a signal passing circuit which constructs the output signals from specific logic level transitions present in the ENABLE input signal. Becerra, 8:60-9:7 and Figure 8.

Further in Becerra, two end cells 98 supply initial tokens for both the main token and the prepulse token inputs to either the BANK 1 cell 100 or to BANK 32 cell 100 depending on the direction of operation being determined by the DIR N and DIR P signal lines. The DIR N/P lines

are set to operate the bank selection shift register 90 from BANK 1 to BANK 32. Becerra, 12:12-12:17 and Figure 9.

Edelen

Edelen discusses latching serial data in an ink jet print head. In Edelen, the loading circuit 10 includes a serial shift register 14 consisting of N number of single-bit storage registers $R_1 - R_N$, such as D, S-R, or J-K flip-flop circuits. Each bit register $R_1 - R_N$ has a data input D, a data output Q, a clock input CLK, and a clear input CLR. To form the serial shift register 14, the data input D of each of the bit registers $R_2 - R_N$ is connected to the data output Q of the adjacent preceding bit register $R_1 - R_{N-1}$. The data input of the bit register R_1 is connected to the serial data line SD. The clock inputs CLK of each of the bit registers $R_1 - R_N$ is connected to the clock line CL1. Edelen, 2:45-2:56 and Figure 1.

Morita

Morita discusses a thermal ink-jet head and recording apparatus. In Morita, the 4-bit shift register 21 and the 32-bit bidirectional shift register 24 are reset by the FCLR signal. When these registers rise, the latch circuit 23 latches the DIR signal, whereby the shifting direction of the 32-bit bidirectional shift register 24 is determined. Then image data is output as the DAT/DIR signal and the BIT SHIFT signal is input as a clock signal for the 4-bit shift register 21. For example, the image data are sequentially taken into 4-bit shift register 21 when the BIT SHIFT signal rises. When the 4-bit image data is taken in, it is latched in the latch circuit 22 when the ENABLE signal rises. The image data thus latched is fed into the AND circuit 25. Morita, 10:50-10:61 and Figure 13.

Claim 1-3

Amended claim 1 recites: "...storing in first memories the firing group data and direction data in synchronization with a shift clock..." Support for this amendment may be found in at least original claim 2. In contrast to claim 1, Becerra does not discuss storing in the first memory the firing group data and direction data in synchronization with a shift clock. This deficiency in Becerra is not cured by Edelen. In Edelen, each of the bit registers $R_1 - R_N$ is connected to the clock line CL1. However, since Becerra is dependent on the timing generator circuit 86 to provide the signals LCLK, PHASE A, PHASE B, SCLK N, and SCLK P, Becerra would be rendered inoperable by the introduction of synchronization with a clock line as discussed in Edelen. As such it is respectfully submitted that the proposed combination of Bercerra and Edelen is improper.

Claim 2 has been cancelled. Claim 3 depends on claim 1 and is therefore believed to be allowable for at least the foregoing reasons. Further, claim 3 patentably distinguishes over Becerra and Edelen, taken alone or in combination. For example claim 3 recites ANDing the nozzle firing signals and the outputs of the nozzle group selection signals of the bi-directional shift register.

Withdrawal of the foregoing rejection is requested.

Claims 4-8

Amended claim 4 recites: "...a selection unit which selects simultaneous firing nozzles based on the simultaneous firing nozzle data and the fire pulse, the selection unit comprising: first memories which store the simultaneous firing nozzle data and the nozzle group firing direction data, the first memories having one more in number than a number of the simultaneous firing nozzles, and second memories which store the simultaneous firing nozzle data, the second memories having a same number as a number of the simultaneous firing nozzles..." Support for this amendment may be found in at least original claims 5 and 6. In contrast to claim 4, Becerra does not discuss that the parallel data latch 80, corresponding to the second memories of claim 4 store the simultaneous firing nozzle data.

Claims 5 and 6 have been cancelled. Claims 7 and 8 depend on claim 4 and are therefore believed to be allowable for at least the foregoing reason.

Withdrawal of the foregoing rejection is requested.

Claims 9-13

Amended claim 9 recites: "...wherein the MSB and the LSB of the bi-directional shift are each initially preloaded with data of "1" prior to the values of the X parallel outputs being shifted." Support for this amendment may be found in at least original claim 10. In contrast to claim 9, Becerra discusses that two end cells 98 supply an initial prepulse token and the main token. In claim 9, a value of "1," corresponding to the token of Becerra, is loaded in to both the MSB and the LSB, which is not discussed in Becerra. Further, this deficiency in Becerra is not cured by Edelen or Morita.

Claim 10 has been cancelled. Claims 11-13 depend on claim 9 and are therefore believed to be allowable for at least the foregoing reason. Further, claims 11-13 patentably distinguish over Becerra, Edelen and Morita, taken alone or in combination. For example, claim 11 recites that values of the X parallel outputs are shifted in a first direction where the additional

bit has a value of 1 and are shifted in a second direction where the additional bit has a value of 0.

Withdrawal of the foregoing rejection is requested.

Claims 14 and 15

Amended claim 14 recites: "...loading a 1 into each of the MSB and the LSB and loading a 0 into each of the X bits as the predetermined value." Support for this amendment may be found in at least original claim 15. Similar to the argument for claim 9, in contrast to claim 14, Becerra only discusses that two end cells 98 supply an initial prepulse token and main token. This deficiency in Becerra is not cured by Edelen or Morita.

Claims 15 has been cancelled. Withdrawal of the foregoing rejection is requested.

CONCLUSION

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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